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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,266	COULSON, RICHARD L.	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8,9,11-15,17-21,23,24,26-35,37,42-46,48,49 and 51-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9,11-15,17-21,23,24,26,27,29-33,35,37,42-45,48,49 and 51-55* is/are rejected.

7)☐ Claim(s) *4,28,34 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 12 – 14, 18, 19, 23 – 25, 31, 35, 37, 51 – 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Emma *et al.* (US Patent No. 6,389,505, hereinafter "Emma").

3. With respect to claims 12, 23, 25, 31, 35, 37, 51 and 56 Emma discloses a memory (figure 2a) comprising:

an area to store data (101); and

an area to store metada for the data (103, 120), the metadata including a plurality of usage bits to indicate usage information for entries in the memory (120, 108), **a** usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a given number of clock periods (213, col. 6, lines 4 – 8, invalid bit indicate whether a cache entry has been accessed during a data retention time period), wherein the memory is a destructive read memory (col. 1, lines 32 – 37) and wherein **a** usage bit for an entry read from the memory is updated during a writeback cycle to write the read entry back to the memory (col. 5, lines 10 – 17, invalid

bit is reset during a refresh or writeback cycle, see also col. 4, lines 46 – 50, the timer is also reset or updated).

4. With respect to claims 18, 52, 54 Emma discloses a system comprising:

a magnetic memory device (figure 1, 40);

a destructive read memory (20) to cache data for the magnetic memory device and to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a give number of clock period (see rejection of claim 12 above); and

a memory controller to update a usage bit for an entry read from the memory during a writeback cycle to write the read entry back to the memory (see rejection of claim 12 above), the memory controller to de-allocate entry using the plurality of usage bits (col. 4, line 67 – col. 5, line 3, modify bit 120 is used when old data is de-allocated or replaced with new data).

5. With respect to claims 13, 19, 24 and 53, the usage information indicates when a memory location was refreshed or used for each location. One of the locations must have been least recently used.

6. With respect to claim 14, the destructive read memory is a cache memory (figure 1, 20).

7. With respect to claim 55, the memory (figure 2, 60) comprises non-volatile memory (40).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 – 3, 5, 6, 11, 15, 26, 27, 29, 30 and 32 – 33 are rejected under 35 U.S.C. 103(a) as being obvious over Ramakrishnan *et al.* (US Patent No. 5,636,355, hereinafter "Ramakrishnan") in view of De Martin *et al.* (US Patent No. 5,619,675, hereinafter "De Martin").

10. With respect to claims 1, 6, 11, 15, 26, 29, 30 and 32, Ramakrishnan discloses a method comprising:

keeping track of least recently used (LRU) information when a memory is accessed to read data (figure 2, 40, 42, 50, reading a dirty block); and

setting a usage bit (dirty block indication) during a writeback cycle to write the read data back to the memory, the usage bit indicating usage information for the read data (23, dirty blocks are purged/writtenback and their dirty indications cleared).

However, Ramakrishnan does not specifically disclose that keeping track of LRU involves checking a current clock period, current clock period being one of a given number of clock periods. On the other hand, De Martin discloses a method to keep track of LRU

information that checks a current clock period (figure 3). De Martin also discloses a different set of usage bits (abstract, claim 2, ICBMs). These bits are set during a writeback cycle in the combined teachings since a writeback operation purges the associated cache entry and consequently the LRU list must be updated.

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan and De Martin before him at the time the invention was made, to use De Martin's method of locating LRU cache line in the computer system of Ramakrishnan to reduce memory overhead (De Martin, col. 2, lines 50 – 3).

11. With respect to claims 2, 3, 27 and 33, see De Martin col. 6, lines 51 – 52. See also claim 2.

12. With respect to claim 5, the memory is a non-volatile cache memory (Ramakrishnan, col. 1, lines 62 – 64).

13. Claims 8, 9, 17, 20, 21, 42 – 45, 48 and 49 are rejected under 35 U.S.C. 103(a) as being obvious over Ramakrishnan and De Martin as applied above and further in view of Davis *et al.* (US Patent Application Publication No. 2003/0023922, hereinafter "Davis").

Ramakrishnan and De Martin disclose all of the limitations of the claims with the exception of a non-volatile destructive magnetic memory. On the other hand, Davis discloses a magnetic random access memory (MRAM), which is a non-volatile destructive magnetic

memory, suitable for both short term and long term storage applications (Davis, col. 1, page 1, paragraph 3).

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan, De Martin and Davis before him at the time the invention was made, to use the MRAM device in the disk cache design of Ramakrishnan and De Martin, since the MRAM devices have relatively low power consumption and relative fast access time, particularly for data write applications, which renders MRAM devices ideally suitable for both short term and long term storage applications (Davis, paragraph 3).

Allowable Subject Matter

14. Claims 4, 28, 34 and 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

15. Claims 32 and 35 have been amended to overcome rejections under 35 USC 101. Corresponding rejections are withdrawn.

Response to Arguments

16. Applicant's arguments filed May 12, 2006, have been fully considered but they are not persuasive. With respect to Applicant's arguments regarding Emma reference, they fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define

a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

17. As to Applicant's argument that "Ramakrishnan did not tech or suggest any writeback cycle to write a block read from a cache to back to the cache", this is not a claimed feature. The claim requires that data read from memory be written back to the memory during a write back cycle. The Examiner agrees with Applicant that Ramakrishnan teaches writing of a data block from a cache to a disk. This reads on the claim because: (1) disk is memory and (2) the disk cache disclosed by Ramakrishnan is populated with data read from the disk which are written back to the disk during purge/write-back cycle.

Conclusion

18. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan
7/10/06

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July 12, 2006

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SUPERVISORY PATENT EXAMINER